TEXAS INSTRUMENTS

Application Report
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54BGA Package

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ABSTRACT

The TI 54-ball low-profile, fine-pitch, ball grid array (TFBGA) meets dimensions specified in JEDEC MO-205, Variation DD. This 0.8-mm-pitch BGA allows economical OEM designs where smaller-pitch 16-bit BGA is either not necessary or is cost prohibitive from a printed circuit board (PCB) fabrication perspective. This BGA is qualified in both the lead (SnPb) and Pb-free (SnAgCu) ball versions at JEDEC Moisture-Sensitivity Level 2/240°C and Level 2/260°C, respectively.

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Widebus is a trademark of Texas Instruments.

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1 Introduction

TI’s new 54-ball low-profile, fine-pitch, ball grid array (LF-XBGA) complies with JEDEC MO-205, Variation DD specifications, offering industry-standard pinouts in both lead (SnPb) and Pb-free package options. This 0.8-mm-pitch BGA enables OEM designers to take advantage of easier, more-economical layouts that are not as costly as smaller-pitch 16-bit BGA packages, with respect to printed circuit board (PCB) fabrication. While not as space-conserving as the 0.65-mm-pitch VFBGA specified in MO-225, this BGA still offers significant space savings, plus thermal and parasitic performance improvements over conventional leadframe-based packaging. This BGA is qualified at JEDEC Moisture-Sensitivity Level 2/240°C for the lead (SnPb) ball and at JEDEC Moisture-Sensitivity Level 2/260°C for the Pb-free (SnAgCu) ball version.

The larger ball allows easier PCB pad-design requirements and enables the package to endure mounted thermal-cycling conditions. The thermal dissipation is slightly better than the smaller 16-bit BGA, and the electrical performance is superior to conventional leadframe-based packages. Package features, characteristics, and performance are defined in this application report.

2 Package Description

2.1 Package Nomenclature

The 54BGA package is available in both SnPb ball and Pb-free ball variations. The SnPb ball package is designated GRD; the Pb-free ball package is designated ZRD. In this application report, “54BGA” is a general reference to the package, independent of ball metallurgy. However, in this application report, references to GRD or ZRD are specific, due to differences in ball metallurgy.

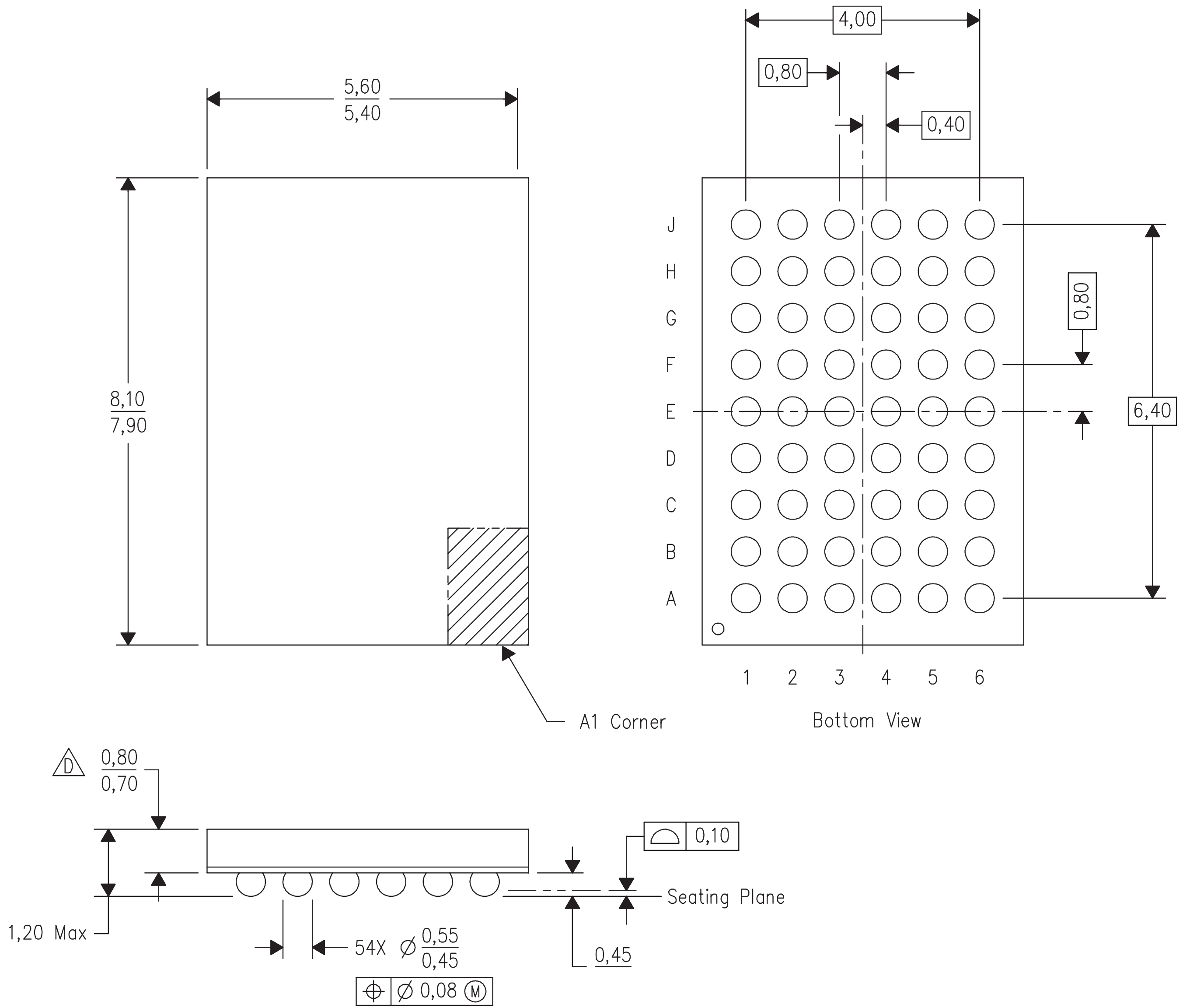
2.2 Package Attributes

Table 1 summarizes the attributes of the SnPb ball (package designator GRD) and the Pb-Free ball (package designator ZRD) 54BGA package. Figure 1 shows the 54BGA package mechanical drawing.

Table 1. Physical Attributes of the 54BGA Package

Attribute	GRD Package	ZRD Package
Pin count	54 (6 X 9 matrix)	54 (6 X 9 matrix)
Square/rectangular	Rectangular	Rectangular
Package length (mm)	8.0	8.0
Package width (mm)	5.5	5.5
Package thickness (mm)	1.2 max	1.2 max
Ball diameter (mm)	0.5	0.5
Ball pitch (mm)	0.8	0.8
Package weight (g)	0.1	0.1
Ball composition	SnPb (63/37)	SnAg1.0Cu0.5
Shipping media, tape and reel (units per reel)	1000	1000
Moisture-sensitivity level	Level 2/240°C	Level 2/260°C

NOTE: All TI Pb-free BGA packages have Z as the first letter of the package designator.



NOTE: SnPb-ball package and Pb-free package have identical dimensions.

Figure 1. 54BGA Mechanical Drawing

2.3 Comparison to Alternative Packaging

Table 2 compares the 54BGA physical attributes to those of alternative package solutions.

Table 2. Comparison of 54BGA to Alternative Packaging Solutions

Attribute	Package					
	56-Pin SSOP (56DL)	48-Pin SSOP (48DL)	56-Pin TSSOP (56PW)	48-Pin TSSOP (48PW)	56-Ball VFBGA (56GQL/56ZQL)	54-Ball BGA (54GRD/54ZRD)
Length (mm)	18.415 ±0.125	15.875 ±0.125	17 ±0.10	14 ±0.10	7 ±0.10	8.0 ±0.1
Width (mm)	10.35 ±0.32	10.35 ±0.32	8.1 ±0.20	8.1 ±0.20	4.5 ±0.1	5.5 ±0.1
Max height (mm)	2.79	2.79	1.2	1.2	1.0	1.2
Pitch (mm)	0.635	0.635	0.5	0.5	0.65	0.8
Footprint (mm^2)	190.6	164.3	137.7	113.4	31.5	44
Weight (g)	0.689	0.604	0.235	0.191	0.0569	0.1
Area savings	76.91%	73.2%	68%	61.2%	<28%>†	—

† The 56GQL package is smaller than the 54GRD package.

2.4 Pinout

The 54BGA pinout is the industry standard for logic devices, and is a direct replacement for competing packages with identical footprints. Figure 2 shows the 54BGA pinout for a standard TI 48-pin Widebus™ function.

	1	2	3	4	5	6
A	Signal	NC	Signal	Signal	NC	Signal
B	Signal	Signal	NC	NC	Signal	Signal
C	Signal	Signal	Vcc	Vcc	Signal	Signal
D	Signal	Signal	GND	GND	Signal	Signal
E	Signal	Signal	GND	GND	Signal	Signal
F	Signal	Signal	GND	GND	Signal	Signal
G	Signal	Signal	V_{CC}	V_{CC}	Signal	Signal
H	Signal	Signal	NC	NC	Signal	Signal
J	Signal	NC	Signal	Signal	NC	Signal

Figure 2. Standard 48-Pin Widebus™ Function Pinout for the 54BGA Package

2.5 Power Dissipation

Thermal performance of the 54BGA is shown in Table 3. This data is modeled, assuming:

- Maximum junction temperature of 125°C
- 105 × 168-mil die size
- Conditions per the indicated JEDEC standard

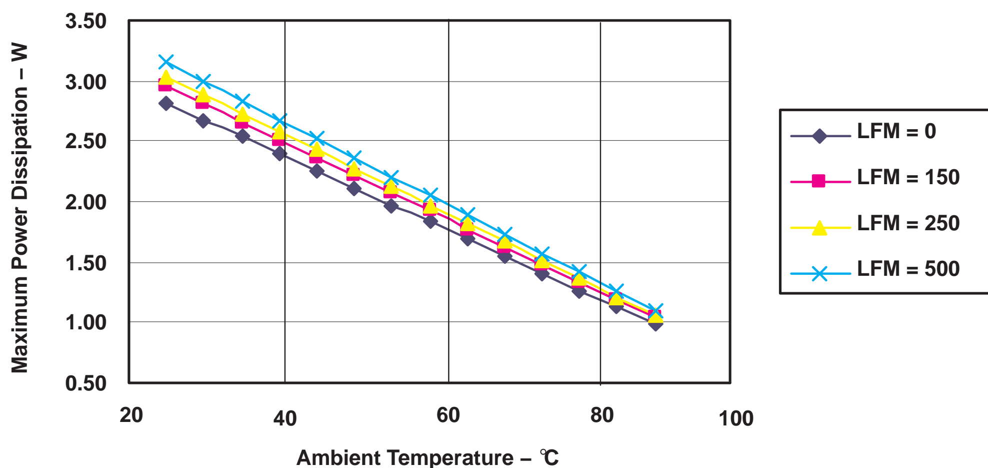
These values represent thermal performance of the package only while mounted to a board per the indicated standard and must not be used to calculate maximum power dissipation in any particular system. To calculate maximum power dissipation in a system, a system-level model must be built and solved. Many factors, such as board construction, number of metal layers and their thickness, die size, board orientation, airflow, altitude, and proximity to other dissipating components or thermal sinks influence power dissipation. The values shown in Table 3 represent a common basis for the relative comparison of the 54BGA to another package's performance. For a complete review of JEDEC standards 51-3 and 51-7 (low- and high-thermal-conductivity boards), see http://www.jedec.org/download/default.cfm for free downloading.

Table 3. Thermal Characteristics of the 54BGA Package

Air Flow (linear feet/minute)	JEDEC Standard	θ_{JA} (°C/W)
0	JESD 51-7	35.5
150	JESD 51-7	33.86
250	JESD 51-7	32.97
500	JESD 51-7	31.77
0	JESD 51-3	64.74
150	JESD 51-3	56.89
250	JESD 51-3	52.85
500	JESD 51-3	47.91
θ_{JC} (junction to case)	19.126	
θ_{JB} (junction to board)	43.36	

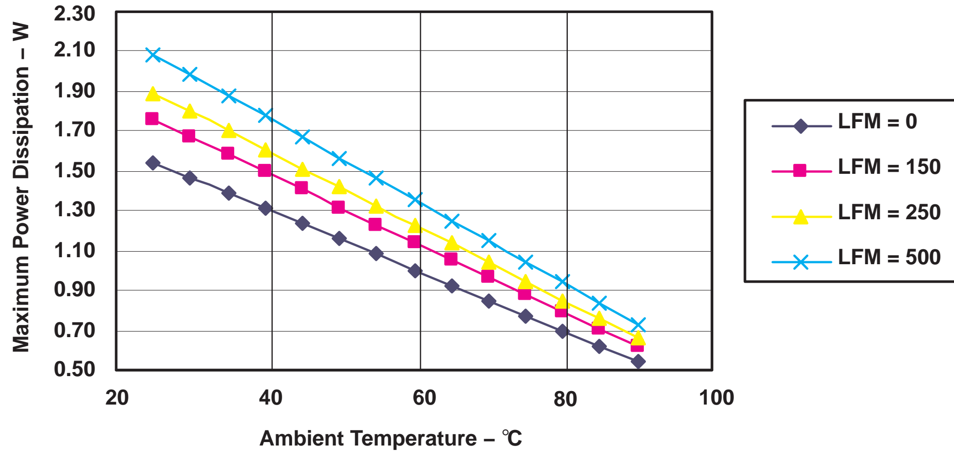
NOTE: Modeled data, assuming 125°C maximum junction temperature and 105 x 168 mil die size

Figures 3 and 4 show the maximum theoretical power dissipation for various airflows per the indicated JEDEC standard. These curves represent the JEDEC test condition only and do not reflect system-level dissipation capabilities. Figure 5 compares the thermal impedance of the 54BGA to alternative packaging.



NOTE: Modeled data, assuming 125°C maximum junction temperature and 105 × 168-mil die size

Figure 3. Power Dissipation per JESD 51-7



NOTE: Modeled data, assuming 125°C maximum junction temperature and 105 × 168-mil die size

Figure 4. Power Dissipation per JESD 51-3

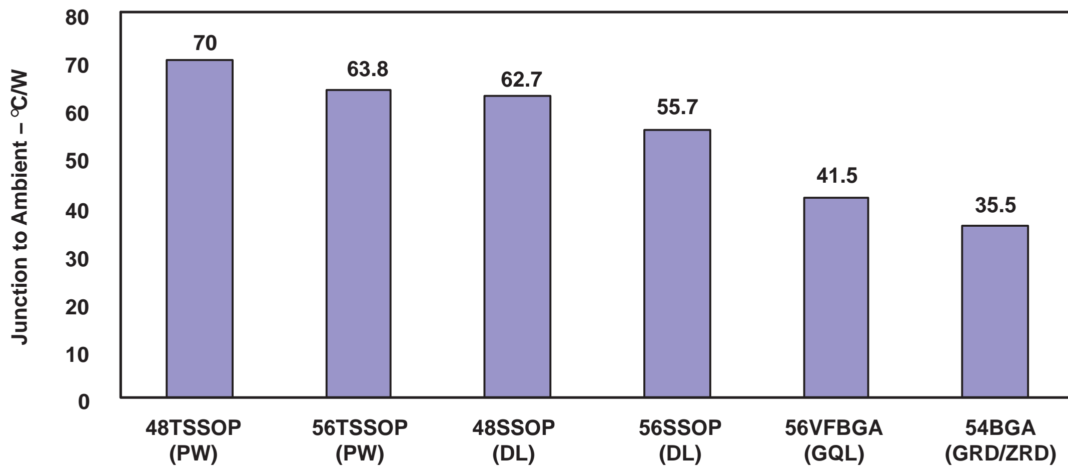


Figure 5. Junction-to-Ambient Dissipation Comparison of Various Widebus Packaging to 54BGA (JESD 51-7)

2.6 Electrical Characteristics

The package parasitics (inductance and capacitance) of the 54BGA are superior to all conventional leaded packages, but are not as low as those of the VFBGA package. Wire lengths in the 54BGA are longer than those of the VFBGA, resulting in slightly increased parasitic values. However, compared to the conventional leadframe-based packages, the improvement is significant. Table 4 compares modeled package parasitics of the 54BGA to alternative packaging. Figure 6 is a graphical representation of the values shown in Table 4.

Table 4. Modeled Electrical Parasitic Values

Package	Resistance (Ω)	Inductance (mA)	Capacitance (pF)
56SSOP	0.055	6.539	0.857
48SSOP	0.048	6.046	0.813
56TSSOP	0.045	3.324	0.564
48TSSOP	0.044	3.019	0.507
56VFBGA	0.065	1.952	0.283
54BGA	0.086	2.383	0.307

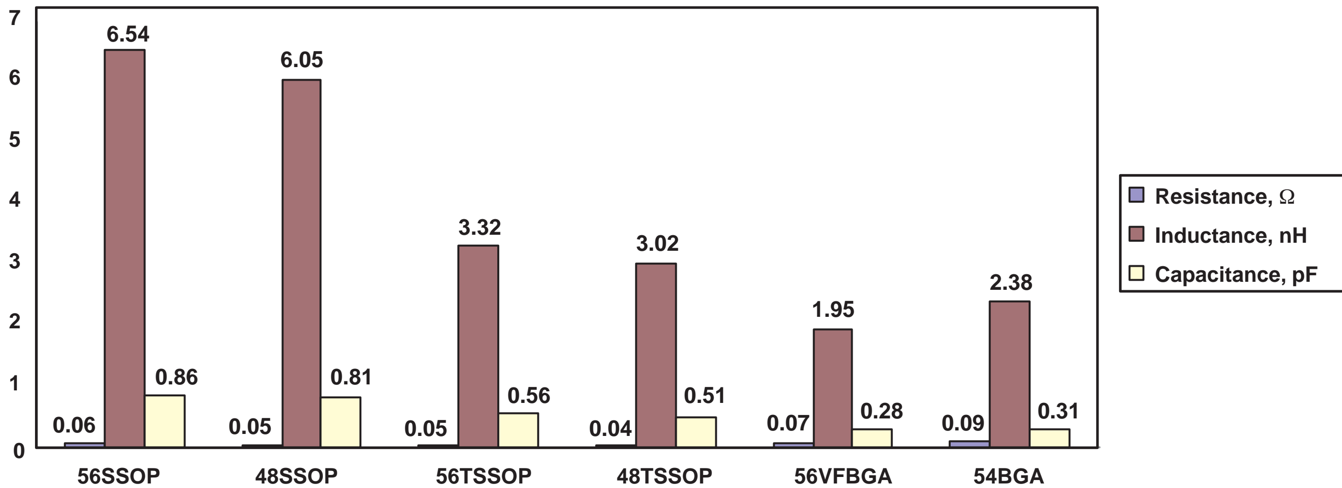


Figure 6. Comparison of Modeled Package Parasitics

3 Package Reliability

The 54GRD is qualified at JEDEC Moisture-Sensitivity Level 2/240°C. The 54ZRD package is qualified at JEDEC Moisture-Sensitivity Level 2/260°C. Table 5 details the reliability testing performed on these two packages.

Table 5. Reliability Testing and Results for 54GRD

Test	Conditions/Duration	Lot 1	Lot 2	Lot 3	Failures
Preconditioning	Level 2 at 240°C +0°C/-5°C	—	—	—	—
†SSLT 150°C	168, 300 hours	40/0	40/0	40/0	0
†Biased HAST 130/85	100 hours	26/0	26/0	26/0	0
†Unbiased HAST	100 hours	77/0	77/0	77/0	0
†Temperature cycling –65°C/150°C	250, 500, 1000 cycles	77/0	77/0	77/0	0
Solderability	Steam age 8 hours	22/0	22/0	22/0	0
Physical dimensions	Per mechanical drawing	5/0	5/0	5/0	0
Flammability	UL94-0	5/0	5/0	5/0	0
	IEC Standard 695-2-2	5/0	5/0	5/0	0
	UL 1694	5/0	5/0	5/0	0
Salt atmosphere	—	22/0	22/0	22/0	0
X-ray	Top side only	5/0	5/0	5/0	0
†Bake 150°C	1000 hours	45/0	45/0	45/0	0
Moisture-sensitivity	Level 2 at 240°C +0°C/–5°C	4/0	4/0	4/0	0
Bond strength	76 balls (min 3 dev)	76/0	76/0	76/0	0
Manufacturability	—	—	—	—	Pass
Visual/mechanical	—	328/0	328/0	328/0	0

† Preconditioned at appropriate level

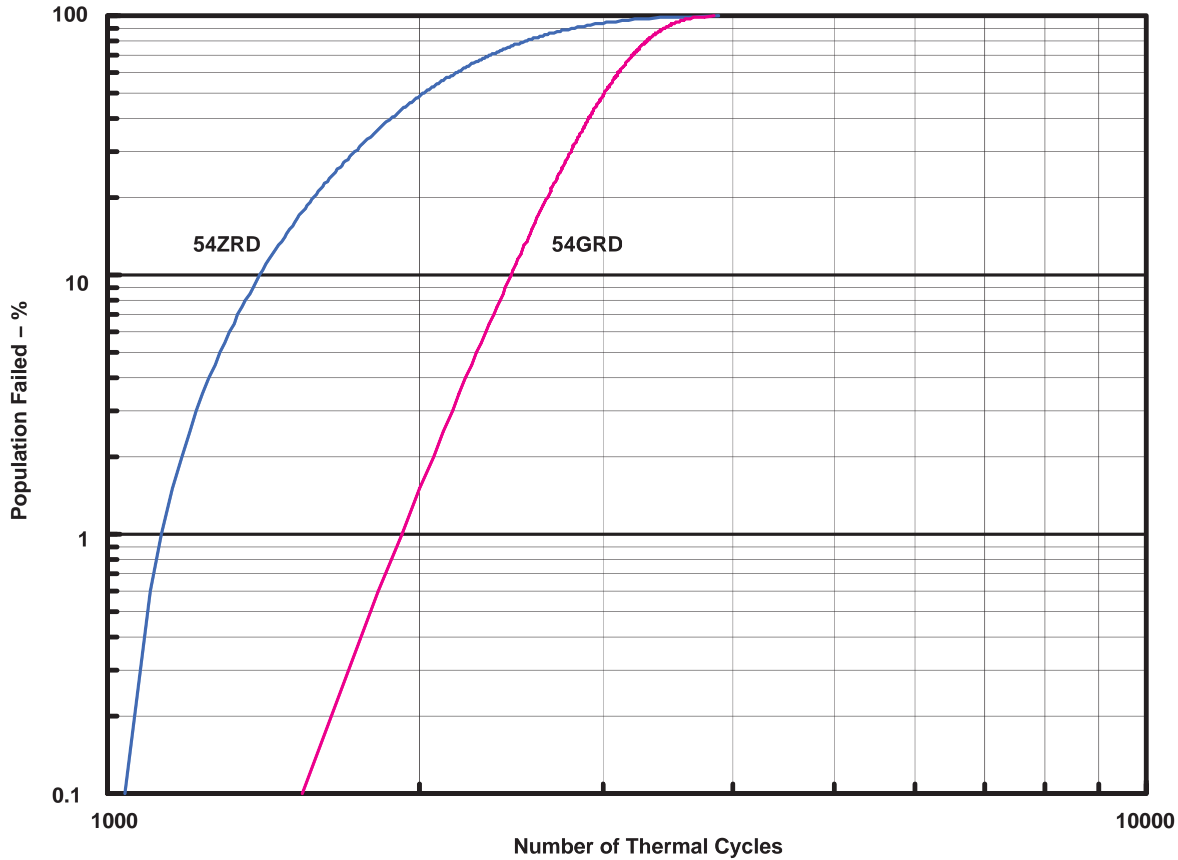
Table 6. Reliability Testing and Results for 54ZRD

Test	Conditions/Duration	Lot 1	Lot 2	Lot 3	Failures
Preconditioning	Level 2 at 260°C +0°C/–5°C	—	—	—	0
†Biased HAST 130/85	100 hours	26/0	26/0	26/0	0
†Unbiased HAST	100 hours	77/0	77/0	77/0	0
†Temperature cycling –65°C/150°C	250, 500, 1000 cycles	77/0	77/0	77/0	0
Moisture sensitivity	Level 2 at 260°C +0°C/–5°C	4/0	4/0	4/0	0
Manufacturability		—	—	—	Pass
Visual/mechanical		328/0	328/0	328/0	0

† Preconditioned at appropriate level

3.1 Board-Level Reliability

The 54GRD and 54ZRD were temperature-cycle tested in the mounted state under a profile that ran from –40°C to 125°C, with 5-minute transition, 10-minute dwell, and 2 cycles per hour. The first failure for both packages occurred past the 1000-cycle point. Figure 7 shows the Weibull distribution of the failures. The Pb-free paste used was Sn/Ag3.9/Cu0.6 on NiAu solder-mask-defined (SMD) pads 0.38 mm in diameter. The SnPb package used OSP/copper SMD pads 0.38 mm in diameter. FR4 epoxy board thickness was 0.8 mm. As noted later in Section 4, nonsolder-mask-defined (NSMD) pads 0.35 mm in diameter would provide better results, but were not tested because SMD provided worst-case conditions.



Package	Cumulative Failures		Average 63.2%	Slope	Least-Squares Fit	Experimental First Failure
	0.10%	1.0%				
54ZRD	1043.37	1130.44	2171.96	2.095	0.9758	1122
54GRD	2007.786	2043.783	3369.73	1.335	0.9737	2021

Figure 7. 54GRD and 54ZRD Mounted Temperature-Cycling Results

4 PCB Design Guidelines

The 54GRD and 54ZRD employ an economically scaled pad design that allows layouts that are less demanding from a PCB fabrication perspective (but use more space) than VFBGA layouts. The preferred pad definition is nonsolder mask (NSMD), 0.35 mm in diameter; with a 0.50-mm diameter etch out around each pad. The maximum trace width is 0.15 mm, and a 0.30-mm (12 mil) drill hole in a 0.56-mm diameter via pad is recommended. After plating, the via diameter is reduced to approximately 0.254 mm (10 mil). Smaller vias could be used, but at a cost penalty. The trace width never should exceed two-thirds of the pad diameter, otherwise, solder balls could wick off the pad and onto the trace during reflow.

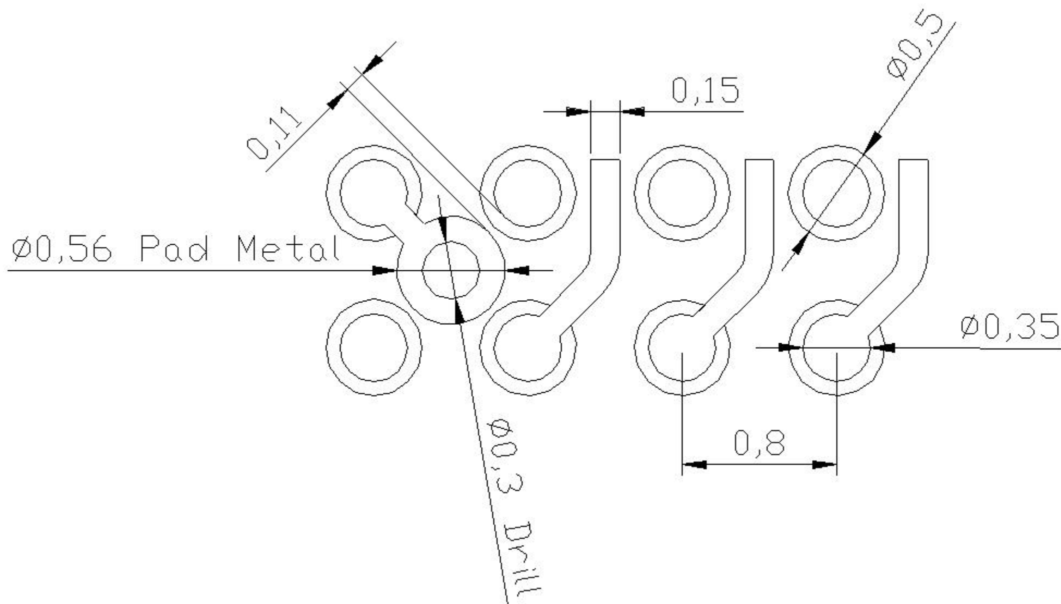


Figure 8. Recommended 54BGA PCB Pad Design

As noted previously, the preferred pad definition is NSMD. The difference between NSMD and SMD is shown in Figures 9 and 10. Note that, at a constant pad diameter, the NSMD offers more solderable area than the SMD because the NSMD pad also allows wetting to the side walls of the pad. The difference in area between NSMD and SMD is equal to πdt, where d is pad diameter, and t is pad thickness. The SMD pad could have an expanded solder mask opening to account for the difference in area, but this can lower standoff height of the package if not properly accounted for with stencil design. Also, the interface between the solderable pad and the mask creates a stress concentration on the solder ball, which could be the initiation point for a fatigue crack (see Figure 10).

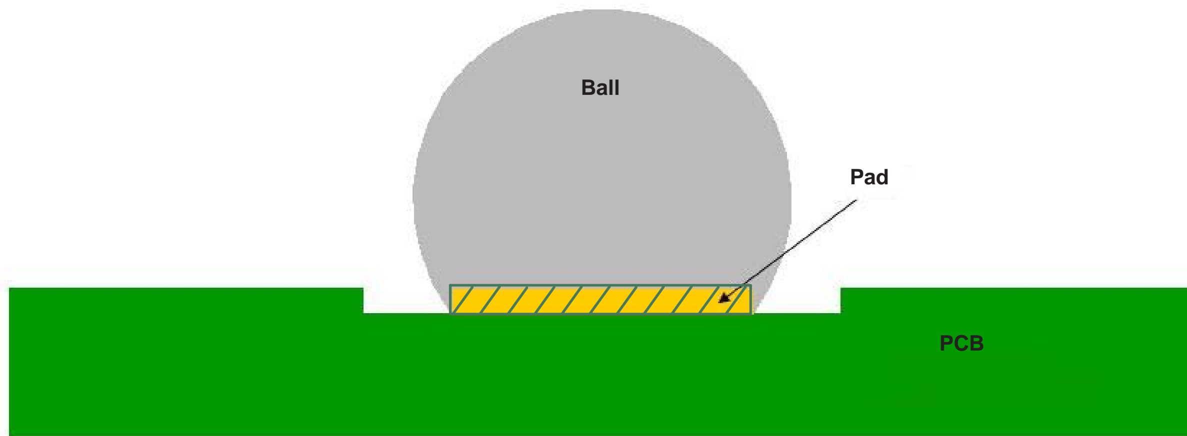


Figure 9. Cross Section of NSMD Solder-Ball Joint

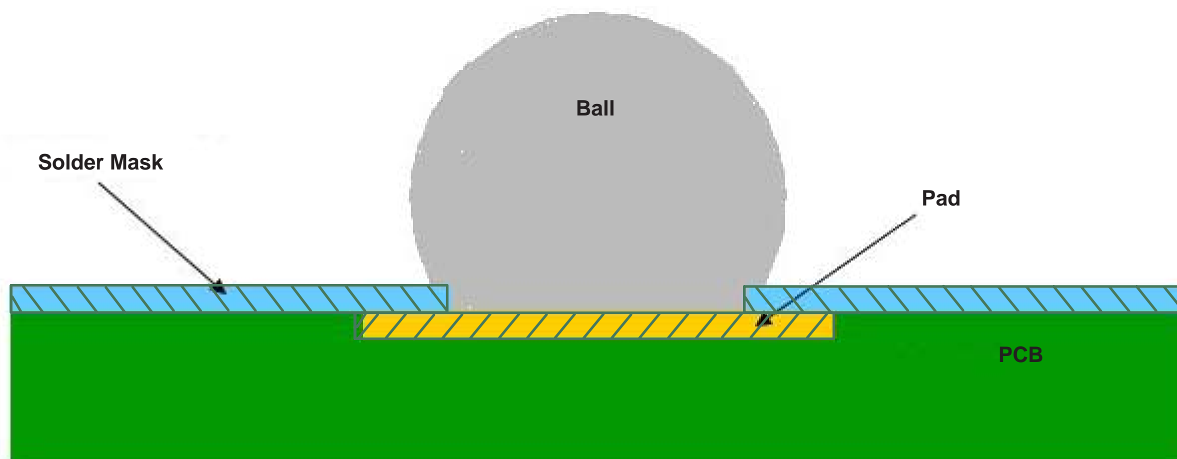


Figure 10. Cross Section of SMD Solder-Ball Joint

5 PCB Assembly Recommendations

The 54ZRD is qualified to JEDEC Moisture-Sensitivity Level 2/260°C, and the 54GRD is qualified to JEDEC Moisture-Sensitivity Level 2/240°C. The selection of a quality type-3 solder paste (or finer grade, if required by other packaging), proper stencil design, and good process control will yield superior results. When developing a reflow profile, target the paste manufacturer's recommended time-temperature targets and do not exceed the JEDEC maximum reflow temperatures cited above. Further process improvements can be made through the use of statistical design of experiments (DOE). The recommended profiles for the two pastes used for internal evaluation are shown in Figures 11 and 12.

The stencil design is an array 0.38 mm square, with radius-cut corners. Chemically etched stencils, while somewhat less in cost, are inferior to laser-cut stencils due to lower transfer efficiency. Laser-cut electropolished stencils offer superior performance in printing and in paste-volume deposition.

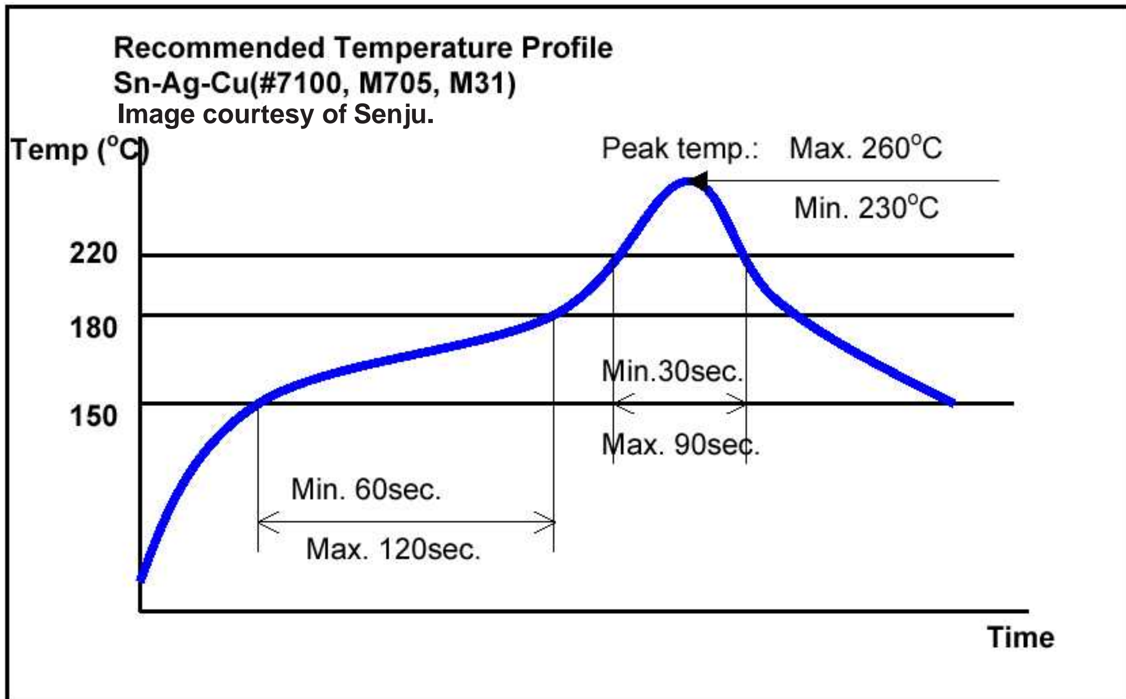


Figure 11. Solder-Paste Manufacturer's Recommended Pb-Free Reflow Profile

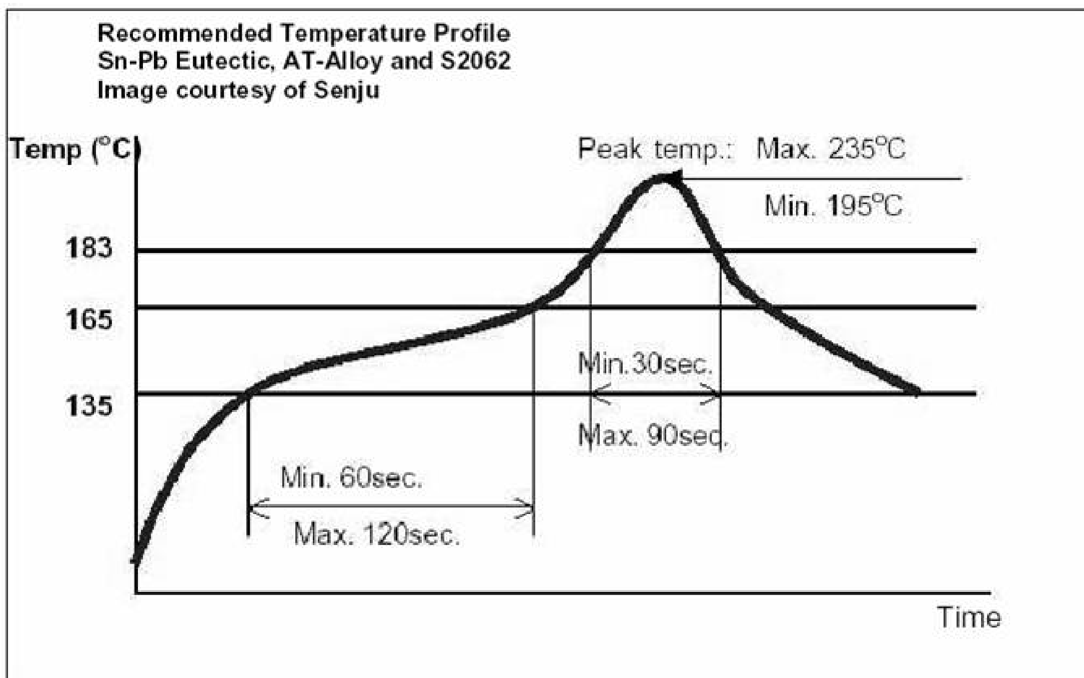


Figure 12. Solder-Paste Manufacturer's Recommended SnPb Reflow Profile

5.1 Rework

BGA rework processes are well defined in industry. The basic elements of this process are:

- Board preheat
- Reflow of component solder
- Vacuum removal of component
- Cleaning and preparation of PCB lands
- Screening of solder paste
- Placement and reflow of new component
- Inspection of solder joints

Several automated rework systems are available and address the previous steps in a variety of ways. One system worth noting is by Air-Vac Engineering (http://www.air-vac-eng.com). The rework steps above (except inspection) can be accomplished with high precision on a single machine under either computer or manual control.

Another example of a well-established rework system is the Metcal APR-5000. This system contains the essential hardware and automated software features necessary for reworking BGA and other packages. This system takes up less than 6 square feet of manufacturing floor space. Both systems offer closed-loop, computer-controlled time, temperature, and airflow parameters help ensure process control and repeatability. The system software manages the reflow profile (preheat, soak, ramp, reflow and cooling). In addition, board temperature can be monitored using three integrated flying thermocouples, and real-time adjustments to all parameters can be made while the profile is running.

A variety of off-the-shelf vacuum collets, nozzles, and solder screens are available from both Air-Vac and Metcal. See http://www.air-vac-eng.com or http://www.Metcal.com for open tools and for custom-tooling requirements.

6 Tape-and-Reel Packing

TI offers tape-and-reel packing for both the 54GRD and 54ZRD packages in standard packing quantities (SPQ) of 1000 units/reel. The units are shipped in embossed carrier tape, sealed with heat-activated or pressure-sensitive cover tape on plastic reels. All of the tape-and-reel materials comply with EIA-481 B and EIA-541. The EIA specifications are shown in Table 7 and Figure 13. The carrier tape is made of conductive polystyrene and has a surface resistivity within the static-dissipative range (1×10^6 to 1×10^{11} Ω/square). Heat-activated or pressure-sensitive, antistatic, clear polyester film is used for the cover tape. The dimensions of most interest to the end user are tape width (W), pocket pitch (P), and pocket size (A_o, B_o, K_o) (see Figure 13).

The units are placed in the carrier tape pocket, with pin 1 located as shown in EIA-481B. The longest axis of the package is perpendicular to the tape sprocket holes, and pin 1 is closest to the round sprocket holes. Thus, for rectangular or square packages, pin 1 is located in quadrant 1. All dimensions are in millimeters.

Table 7. Carrier-Tape Dimensions

Package	Carrier-Tape Width (W)	Pocket Pitch (P)	Pocket Width (A_O)	Pocket Length (B_O)	Pocket Depth (K_O)	Device Quantity Per Reel (SPQ)
54GRD	16.0 ± 0.30	8.0 ± 0.10	5.8 ± 0.10	8.3 ± 0.10	1.55 ± 0.10	1000
54ZRD	16.0 ± 0.30	8.0 ± 0.10	5.8 ± 0.10	8.3 ± 0.10	1.55 ± 0.10	1000

D_O	D_1 Min	E_1	P_O	P_2	R Ref.	S_1 Min.	T Max.	T_{1O} Max.
1.5 +0.1/–0.0	1.5	1.75 ± 0.1	4.0 ± 0.	2.0 ±. 05	30	0.6	0.6	0.1

NOTE: All dimensions are in mm.

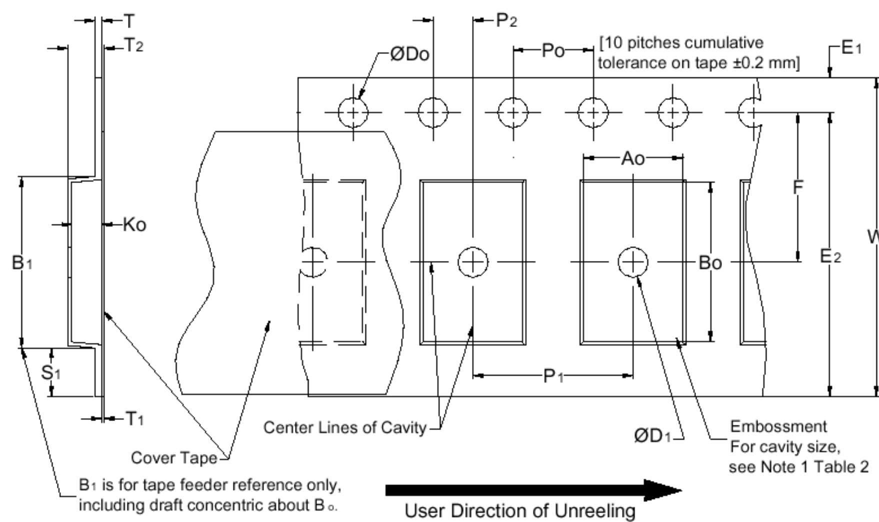


Figure 13. 54BGA Carrier-Tape Drawing

As stated previously, the 54ZRD is qualified at JEDEC Moisture-Sensitivity Level 2/260°C, and the 54GRD is qualified at JEDEC Moisture-Sensitivity Level 2/240°C. These BGA packages are packed in moisture-barrier bags and sealed with desiccant. Floor life (out of the bag) at factory ambient conditions of +30°C/60% RH, or less, is 1 year.

7 Marking

The top of the package is marked by laser with device name, corporate ID, date code, assembly-site code, assembly-lot trace code, and pin 1 location. Table 8 shows the symbolization guidelines for the 54BGA packages.

Table 8. Device-Marking Guidelines

QFN Symbolization Guidelines					
Pins	**Package**	**Namerule and Format**	**Maximum Characters per Row**	**Maximum Rows**	**Symbol Format**
54	GRD	C1	10	2	TI YMLLLLS O LD244A

LD244A = Short device name for SN74LVC16244AGRDR or ZRDR (“R” denotes tape and reel packing)
TI = Texas Instruments
Y = Year
M = Month
S = Site code
LLLL = Lot trace code
O = Pin 1 quadrant identifier (data sheet specifies exact pin 1 location)

For specific marking on any particular device, see the device data sheet at www.ti.com.

8 Test Sockets

Test sockets for 54BGA packaged devices can be obtained from:

Plastronics
2601 Texas Drive
Irving, Texas 75062
Phone: 972-258-2580
Fax: 972-258-6771

Socket part number: 054UG08C127

9 Features and Benefits

In summary, key features and corresponding advantages for logic products in the 54BGA package are:

- Superior package parasitics compared to traditional dual-in-line packaging solutions. Inductance ranges from 63% to 21% lower than alternative packages, and capacitance ranges from 64% to 39% lower than other comparable packages.
- Superior thermal performance and board-level reliability compared to alternative package solutions. 54BGA junction-to-ambient thermal impedance ranges from 49% to 36% lower than conventional leadframe-based packages.
- Economical PCB layout requirements and fabrication costs
- Available in either Pb-free or SnPb options

- Significant area savings over traditional dual-in-line packages. 54BGA is 61% to 76% smaller than its equivalent-pin leadframe-based counterpart.
- Thinnest package available within JEDEC MO-205, Variation DD

10 Conclusion

Texas Instruments 54GRD and 54ZRD packages are leadframe-based leadless packages, with improved thermal performance, electrical performance, and package volume compared to similar TSSOP, TVSOP, SSOP, and SOIC packages. Additionally, the 54BGA packages meet the industry's lead-free demands, have reliable solderability with either the Pb or Pb-free package options, and can be manufactured and reworked using conventional equipment. The packages allow product miniaturization and comply with dimensional specifications of JEDEC standard MO-205, Variation DD.

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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