



Advanced Test Technologies

### Minimizing Socket & Board Inductance using a Novel decoupling Interposer

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James Zhou, Hongjun Yao

- It is better to uncover a little than to cover a lot.

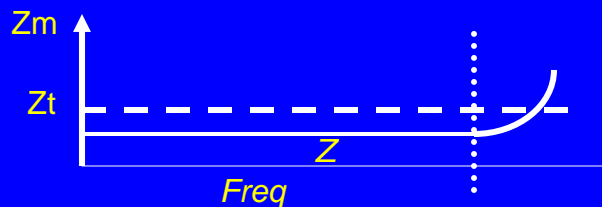
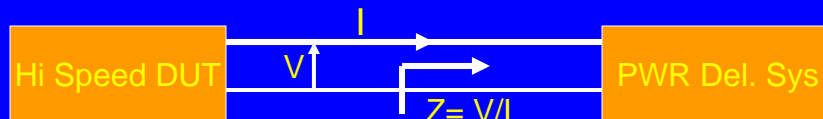
- *Eric Bogatin* , SI Artisan  
» [www.bethesignal.com](http://www.bethesignal.com)

## Performance Limiting Noise

- Power ground voltage droop (Rail Collapse)
- Simultaneous Switching Noise (SSN – Ground Bounce)
- PDS Components
- Board – Socket – DUT package – decoupling components

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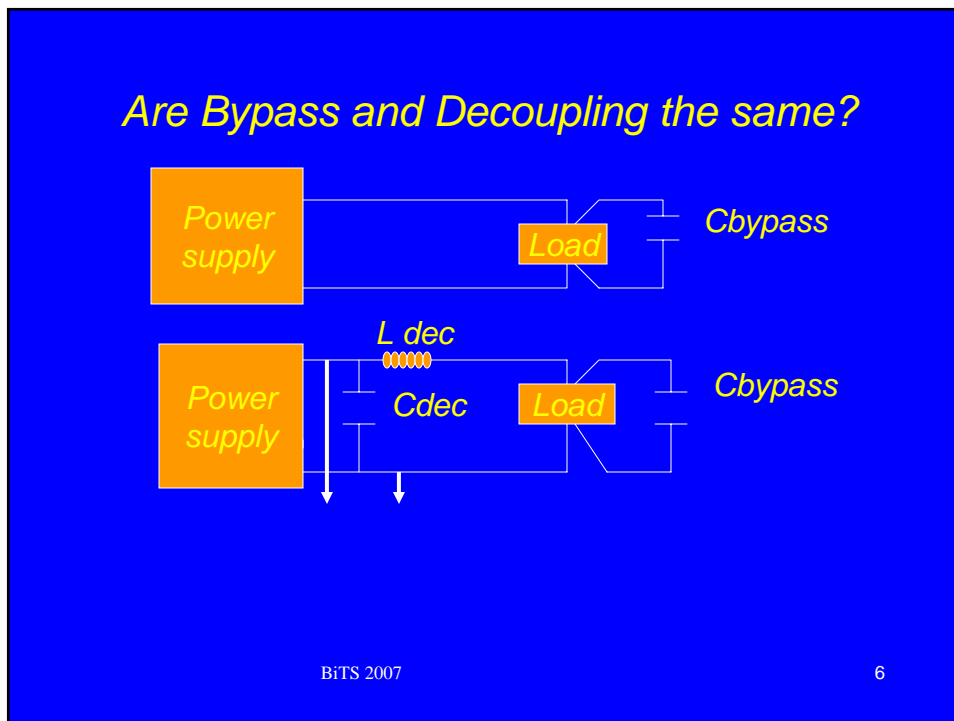
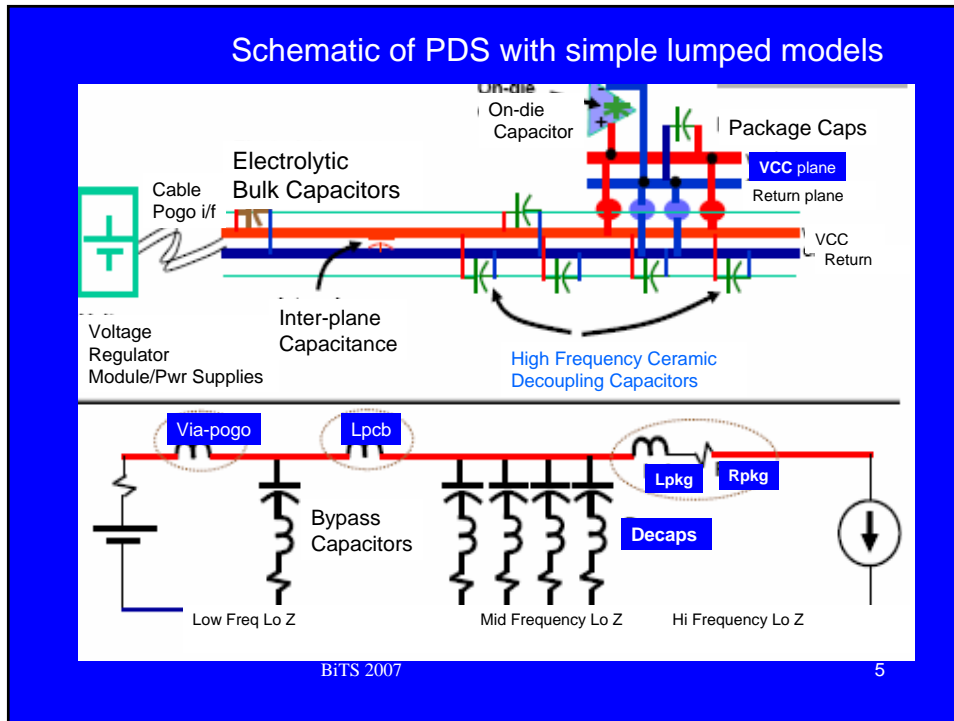
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*PDS has to distribute the power to the chip  
Has to keep the ripple (noise) to spec ~ 5%  
Can not droop all the way to the BW of DUT*

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### Basic PDS Design Strategy

Determine required PDS impedance

$$Z = \Delta V / \Delta I$$

Determine the frequency for the PDS alone

$$F_{pds} = Z / 2\pi L_{pds}$$

$$\text{Bypass } C = 1 / 2\pi F_{pds} Z$$

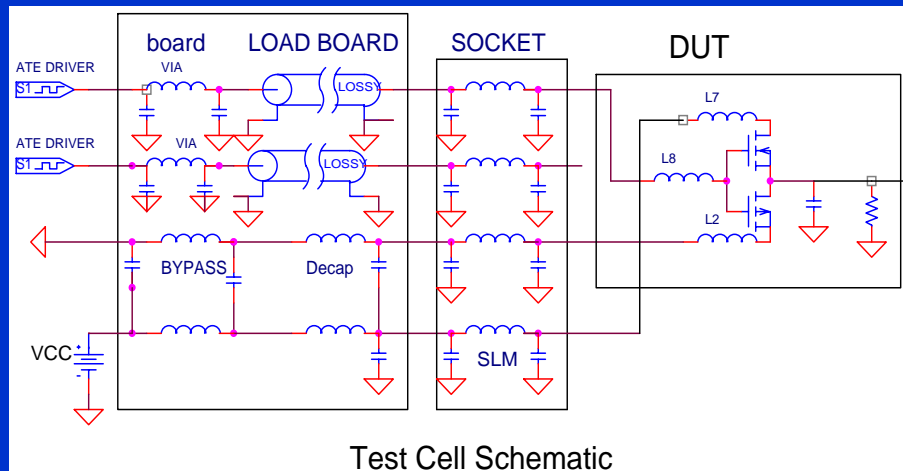
Determine how much L we can handle at Fmax

$$L = Z T_r / \pi$$

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### Reviewing SSO/SSN/Ground Bounce



Test Cell Schematic

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FIGURE. A

$$\frac{V_{gb}}{V_s} = n \times \frac{L_{net}}{T_r \times Z_o}$$

*3 nets, 5nH, 0.5ns Tr, 50 ohms  
60% Vgb!*

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## Inductance is like Kryptonite!

- For Digital Designers of high speed test cells,
- Inductance is the bane of good designs

Capacitance is like Free Beer!

### *Simulation of the impact of Bypassing*

- 8 layer FR4 board; 0.635mm dielectric
- 5 .01uF caps on bottom of the board
- 1 power via; .25mm dia.; 0.5mm antipad
- Chip mounted directly to the board
- Chip in a socket mounted to the board
- Chip in a socket with the .01uF caps

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### *Load Configuration*

- 10 ohm resistive load to draw 100ma
  - from 1v supply
- 0.1nF on chip bypass on each power pin
- Load is turned on at 5ns,
  - the Tr is 200ps

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### Spring Pin and Load Model

- Spring Pin is modeled as a CLC pi network
- There is a 10nF bypass in the interposer

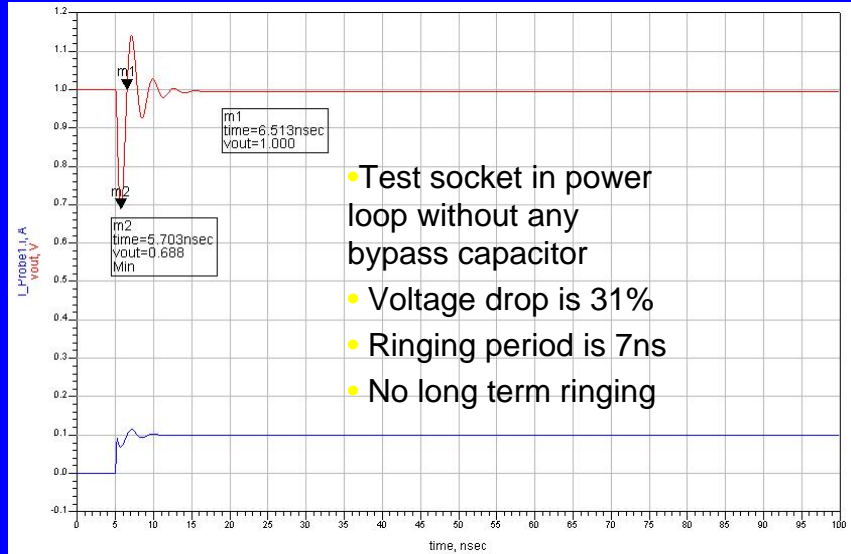
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### Case 1. Chip mounted to the PCB

- Test socket not in power loop
- Voltage drop is 22%
- Ringing period is about 5ns
- No long term ringing on power net

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*Case II: Using Socket with no bypass*

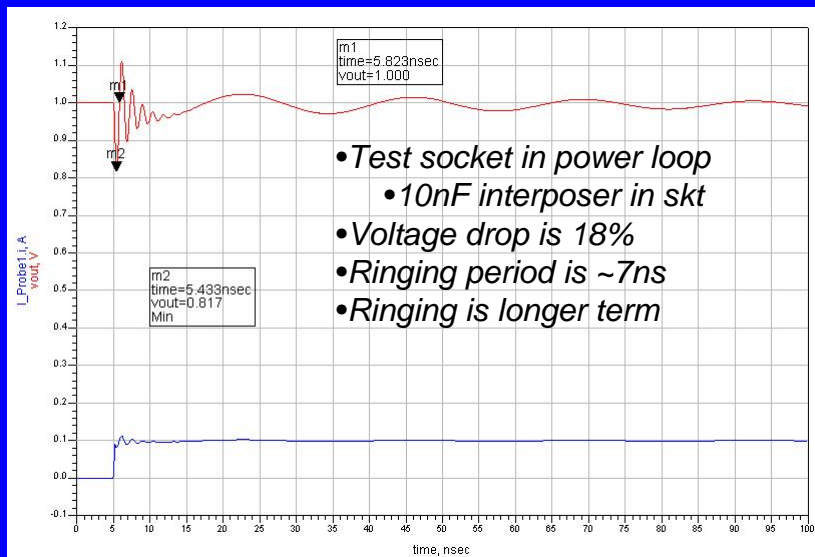


- Test socket in power loop without any bypass capacitor
- Voltage drop is 31%
- Ringing period is 7ns
- No long term ringing

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*Case III: Contactor with bypass interposer*



- Test socket in power loop
  - 10nF interposer in skt
- Voltage drop is 18%
- Ringing period is ~7ns
- Ringing is longer term

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## Observations

- 1nH test contactor increases the power drop from 22% to 31%
- 10nF bypass cap reduces the power drop to 18%
- The built-in bypass cap and the spring pin inductance causes some long term ringing on the power net..

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## Interposer Position

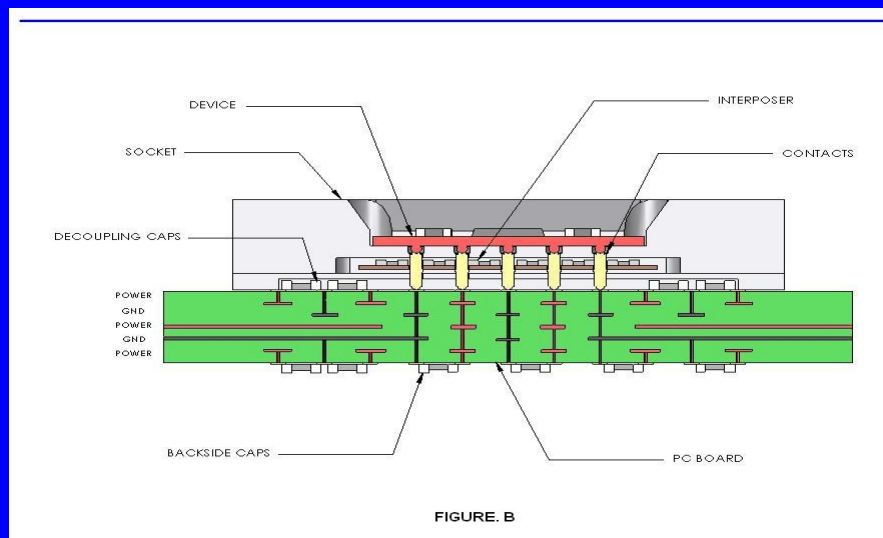
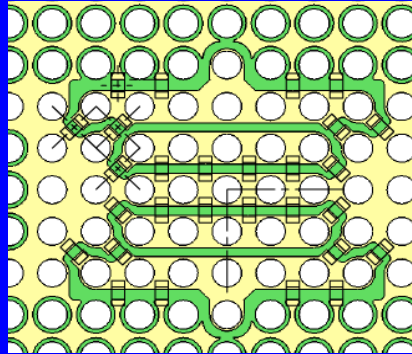


FIGURE. B

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## Decoupling Interposer



Drawing of Interposer

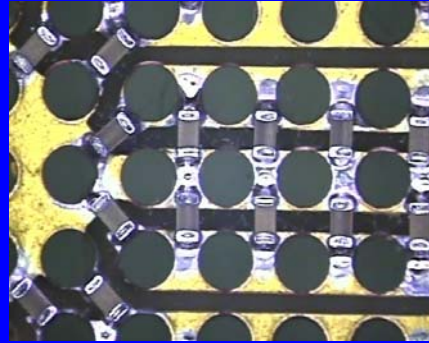
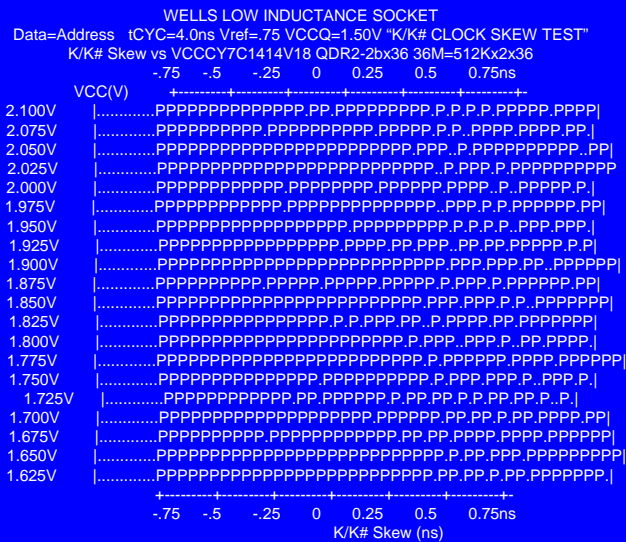


Photo of Interposer – 1mm pitch

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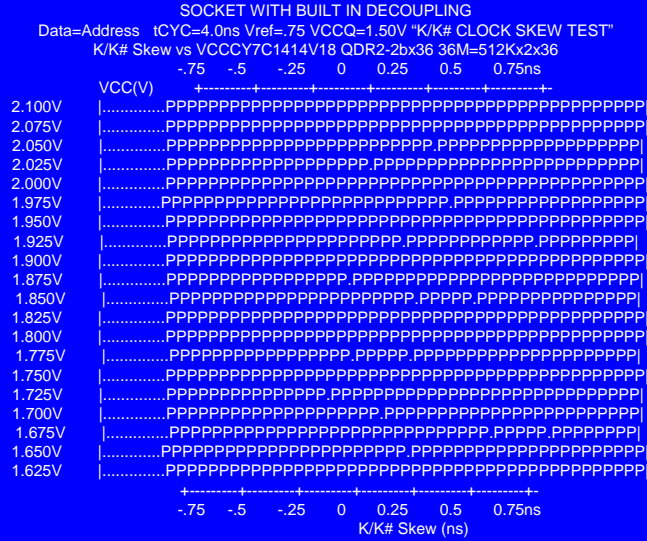
## Socket without Built-in Decap



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## Socket with Built in Decoupling



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## Summary

- Inductance is the number one cause of noise and the primary cause of rail collapse
- A well designed cap network will counteract the Inductance
- The closer the caps to the noise source; the more effective they are
- Thanks to Cary Stubbles of Cypress for his support.

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